Preprint
UCRL-JC-149976

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This article was submitted to :
International Workshop on Recent Progress of Induction Accelerators
Tsukuba, Japan, Oct 29-31, 2002

U.S. Department of Energy
Lawrence Livermore National Laboratory

December 4, 2002

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Abstract

The Beam Research Program at Lawrence Livermore National Laboratory (LLNL) has been developing solid-state modulators for accelerator applications for several years. These modulators are based on inductive adder circuit topology and have demonstrated great versatility with regard to pulse width and pulse repetition rate while maintaining fast pulse rise and fall times. These modulators are also capable of being scaled to higher output voltage and power levels. An explanation of the circuit operation will be presented along with test data of several different hardware systems.

I. BACKGROUND

As the performance of solid-state devices, specifically MOSFETs and IGBTs, improve with regard to their power handling capability and turn-on/turn-off times, these devices are replacing hard vacuum tube devices [1]. At LLNL this effort began more that a decade ago with the goal of developing modulators to provide high-voltage pulses for linear induction accelerator applications. These early modulator designs use high-voltage, high-current switches composed of series/parallel arrays of MOSFETs to drive pulse transformers arranged into an adder configuration. The Advanced Radiograph Machine (ARM) modulator, was the first LLNL high power pulser specifically developed to show feasibility of using solid-state adder-type modulators to drive induction accelerator cells [2] and successfully demonstrated the capability and flexibility of the circuit topology. ARM, designed to generate a burst of 45kV pulses at peak currents exceeding 5kA, was capable of generating pulses having an output pulse-width that could be continuously varied between 200ns and 1.5μs. These pulses with rise and fall times of <100ns could be generated at burst frequencies exceeding 1MHz. Having demonstrated the capability of the basic technology, development of solid-state switched inductive adder circuits has continued in meeting the requirements of other applications.

This paper discusses the design and performance of several different pulsers having a wide range of requirements. Two of the applications are for fast kicker pulsers where very fast rise and fall times are essential. The other end of the spectrum is a slower but very high power modulator designed to drive klystrons. The solid-state device needed for each of these applications is different with regard to peak power capability and switching speed but share key similarities that allow them to work in this very versatile circuit topology.

II. CIRCUIT TOPOLOGY

In the basic adder configuration shown in Fig. 1, the secondary windings of a number of 1:1 pulse transformers are connected in series. Typically, for fast pulse applications, both the primary and secondary winding consists of a single turn to minimize the leakage inductance. In this configuration, the output voltage on the secondary winding is the sum of all the voltages appearing

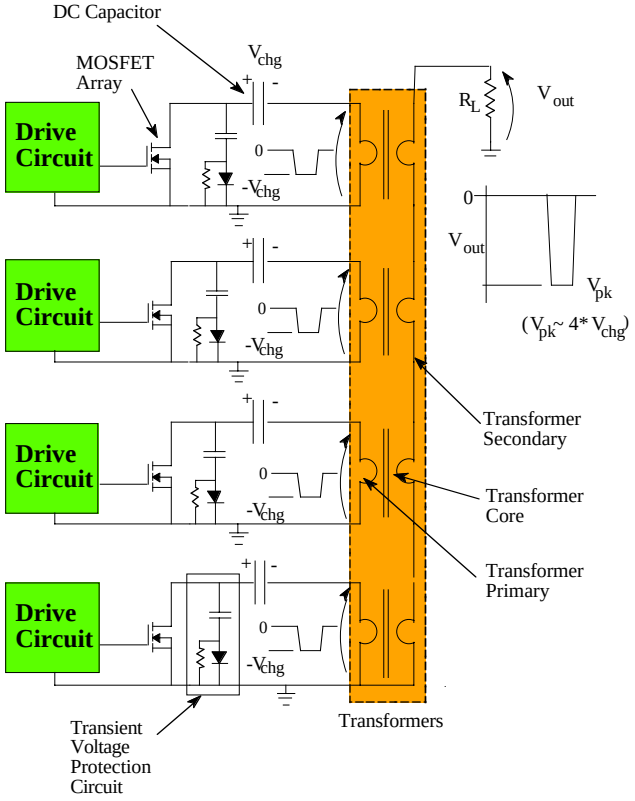

Figure 1. Simplified Schematic of Adder Circuit – Four Adder Cells Shown

*This work performed under the auspices of the U.S. Department of Energy by University of California Lawrence Livermore National Laboratory under contract No. W-7405-Eng-48.

on the primary windings. The adder circuit topology has certain advantages as well as issues:

Advantages:

- All drive components ground referenced
- No high-voltage grading of components required
- Output pulse format defined by programmable pulse generator and provides the capability of:
  - -Pulse width agility
  - -Burst frequency agility
  - -High burst frequency: >5 MHz
- Modular – consists of identical modules
  - -All modules switch same current
  - -All modules triggered simultaneously
  - -Scaleable to higher voltages by adding modules
- Low source impedance
  - -Can drive wide range of load impedance
  - -Load voltage is essentially independent of load

Issues:

- Each module must switch full load current
  - -May require many parallel components
  - -Parallel switching devices must have low jitter on both turn-on and turn-off
- Requires very small loop inductance
- Requires very fast opening switch that can interrupt full load current and survive fault currents
- Fault currents can be very large
- Cost

The key element in this circuit topology and the component that provides exceptional flexibility and capability is the solid-state switching device used in the primary side of the transformer circuit. These devices must be very fast and be capable of being easily controlled during both turn-on and turn-off. Until the development of high-power MOSFETs and IGBTs these requirements could only be met with vacuum tube devices such as planar triodes and other grid-controlled high power vacuum tubes. While vacuum tube devices are more easily operated in their linear region than solid-state devices, their internal impedance is much higher and overall efficiency is much lower. This linear capability is not often needed as most accelerator applications require rectangular pulse having minimum voltage ripple on the flattop, and these requirements are efficiently satisfied by solid-state devices that turn-on to a very low source impedance. When pulse waveshapes other than rectangular are needed, the flexibility of the inductive adder circuit topology allows some level of waveshape modulation.

In the primary-side circuit (Fig.1), the source impedance of the solid-state switch (shown as a MOSFET array for this discussion) and the DC capacitor bank must be very low ($<<1\Omega$). A small source impedance is required to be able to provide the total drive current (secondary current, any additional current loads in the primary circuit, plus the magnetization current for the transformer core) without excess voltage droop during the pulse. The physical layout for this circuit is critical, as it is necessary to minimize total loop inductance (consisting of the loop area formed by the switch, capacitor, and transformer). Voltage drop across a loop inductance larger than 5-10 nanohenries can significantly degrade circuit performance when the di/dt is greater than 10kA/μs. Loop inductance can be minimized and controlled by mounting the components on printed circuit boards (pcb), using wide copper traces and placing the supply and return current paths on opposite sides of the pcb.

The MOSFETs shown in the simplified circuit schematic in Fig.1 have their source lead connected to ground. This is chosen so that all the gate drive circuits are also ground referenced, thereby eliminating the need for floating and isolated power supplies. The pulse power ground and the drive circuit ground have a common point at the MOSFET source connection but otherwise do not share common current paths; thereby reducing switching transients being coupled into the low-level gate drive circuits.

Excessive voltage transients can be generated across the solid-state device during fast turn-off. Transients are the result of energy stored in the stray loop inductance, energy stored in the transformer primary, and/or voltage coupled into the primary circuit from the secondary (usually due to fault condition or trigger timing differences in stages of the adder). Transient protection for the MOSFETs is provided by the series combination of snubber capacitor and diode tightly coupled to the MOSFET (Fig.1). The capacitor is initially charged to the same voltage as the DC capacitor bank. When the MOSFET is turning on, the diode prevents the snubber capacitor from discharging through the MOSFET. As the MOSFET turns off, transient voltages that exceed the voltage on the snubber capacitor turn the diode on so that the capacitor can absorb the excess energy. A resistor in parallel with the diode allows the excess capacitor energy to discharge into the DC capacitor between bursts. Good performance of the over-voltage circuit requires a low inductance capacitor and a diode with a low forward recovery voltage.

Not shown in the simplified adder circuit layout is the reset circuit for the magnetic cores. The cores require reset so that they do not saturate during a voltage pulse. If this circuit operates in a pulse burst format or if the interval between pulses is long, a DC reset circuit can be used and is implemented by connecting a DC power supply through a large isolation inductor to the ungrounded end of the secondary winding of the adder stack. In the long interval between bursts or for low duty cycle pulses, the reset current will reset and bias the magnetic cores. This approach is simple to incorporate and requires few additional components but has the disadvantage of requiring the transformer to have sufficient magnetic core material to sustain the entire burst stream. When the cores must be reset quickly between pulses, active (pulsed) reset applied to either the primary or secondary side of the transformer is often used. Active reset circuits are more complicated than DC reset and usually require a controlled switch, charged capacitor, timing/trigger pulse and associated control circuitry as well as some circuit element to isolate the reset circuit from the high-voltage pulse.

III. DEVICE EVALUATION AND SELECTION

The applications' requirements determine the specific solid-state device(s) that can be used. For a fast dipole kicker pulser having the requirements shown in Table 1,

Table 1. Pulser Performance Requirements

Parameter	Requirement
Output Voltage	20kV into 50Ω
Voltage Rise/Fall-time	≤10ns (10-90%)
Flattop Pulse-width	20ns–200ns(continuously adjustable)
Burst Rate	4pulses@1.6MHz(~600ns between leading edges)

the selection process detailed in the following discussion chooses a solid-state switching device.

The key parameter in this performance requirement is the minimum pulsewidth of 20ns. As a class of devices, 1kV rated MOSFETs have demonstrated the required rise and falltime; however, the critical information needed was a determination of whether MOSFETs are capable of switching significant current while simultaneously achieving the required minimum pulsewidth. Device datasheets do not necessarily provide all the information required to make a definitive decision: testing is essential.

In order to keep the total number of devices required to a reasonable value, it is important to minimize the number of series elements. Therefore only MOSFETs capable of operation at voltages of ≥ 700 volts were considered for testing. The MOSFET evaluation circuit was a series circuit consisting of a low inductance DC capacitor bank, a resistive load, and the MOSFET. Devices were evaluated on the basis of switching speed (turn-on and turn-off) at various peak currents, overall waveshape, minimum achievable output pulsewidth, and ease of triggering. Extensive testing of many devices from several vendors produced several that were acceptable and led to the selection of the APT1001RBVR. During testing, this device exhibited the cleanest rise-time and fall-time and met the pulsewidth, risetime, and falltime requirements. We were also able to measure a peak current of ~35 amperes before seeing an unacceptable drain-source voltage drop (we arbitrarily chose a voltage drop of < 20 volts during conduction of the current pulse as our acceptance criteria). The APT1001RBVR has a 1000V maximum drain to source rating, an average current rating of 10A, and a pulsed current rating of 40A. This device is available in a standard TO-247 package.

During the early testing of MOSFETs, it was apparent that the MOSFET gate drive circuit was also an essential element in achieving the best performance from the individual devices. The coupling between the drive circuit and the MOSFET had to have very low loop inductance, as the peak drive current required to achieve fast switching performance was on the order of tens of amperes. Even the devices within the gate drive circuit had to be very fast and have short turn-on and turn-off delay times. An early decision was that each MOSFET would require its own dedicated gate drive. A simplified schematic of the drive circuit is shown in Fig. 2. The input device of the gate drive has a level shifting TTL input circuit internally coupled to a MOSFET totem pole output. This circuit drives a fast, high current MOSFET (peak current ±20 amperes) totem pole device which drives the gate of the power MOSFET (capacitive load) to turn it on and sinks current from the MOSFET to turn it off. The gate drive circuit components require a DC voltage of ~ 15 volts. For longer duration pulses, commercially available MOSFET drivers provide adequate performance but tight coupling between the driver and MOSFET is still required.

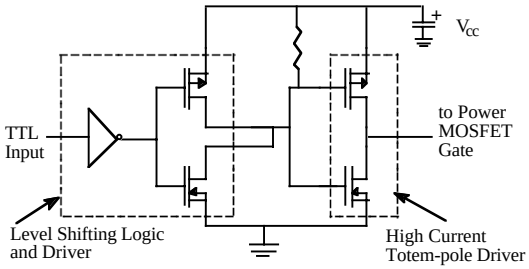

Figure 2. Simplified Schematic of MOSFET Drive Circuit

IV. TRANSFORMER DESIGN AND COMPONENT LAYOUT

The adder transformer is designed to look very much like an accelerator cell of a linear induction accelerator with the primary winding totally enclosing the magnetic core (an annealed and Namlite insulated Metlgas® 2605 S1A tapewound toroid purchased from National/Arnold). The geometry (specifically, the cross-sectional area) of the magnetic core is based on the volt-second product required to satisfy the pulse or burst requirements of the application. It is always prudent to have more material than is required to satisfy the minimum pulsewidth requirements (a saturating single-turn transformer is a very low impedance load and very large currents are possible). As shown in Fig. 3, the input drive connection between the transformer primary and ground has sliding contacts that make electrical connections to a printed circuit board (pcb) when the pcb is inserted between the contacts. Two boards (designated MOSFET carrier boards) are inserted into the transformer from opposite sides. Modules of this configuration are stacked (toroid center axis vertical) to form the adder with the number of modules determining the final output voltage.

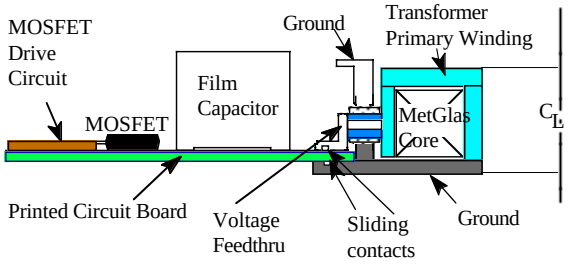

Figure 3. Simplified Cross-Section of the Pulse Transformer with PCB Inserted

Each MOSFET carrier board is laid out to have six pairs of MOSFETs symmetrically arranged in a circular pattern such that identical current paths exist. Controlling total loop inductance for each MOSFET ensures that all

devices switch the same peak currents. Also mounted on the pcb are the MOSFET gate drive circuits, the DC storage capacitors and the snubber circuits. Each module has a total of 24 MOSFETs which gives a comfortable margin in peak current capability that allows for extra loading in the primary circuit, a reasonable magnetization current, and total load current. A photograph of one MOSFET carrier board inserted into a transformer assembly is shown in Fig. 4. The gate drive circuit boards (one dedicated to each MOSFET) receive their trigger pulses from a single trigger circuit (also mounted on the MOSFET carrier board) which is connected to an external pulse generator by coaxial cable.

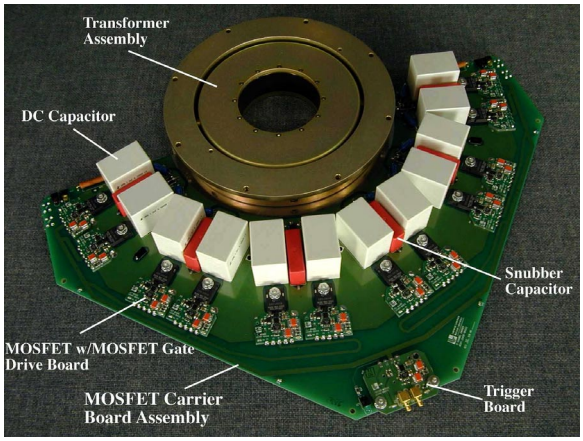

Figure 4. Transformer Assembly. With One MOSFET Carrier Board Inserted

A complete prototype kicker adder assembly consisting of a stack of transformer assemblies bolted together is shown in Fig. 5. The MOSFET carrier boards are shown inserted into the transformer assemblies. This modular configuration is intended to allow for easy maintenance: in the event of a component failure, the entire board can be replaced in minutes. The secondary winding for the pulser is usually a metal rod that is positioned on the axial centerline of the adder stack. The rod may be grounded at either end of the adder stack to generate an output voltage of either polarity. The 50Ω high-voltage output cable enters the pulser from the top of the enclosure.

V. FAST DIPOLE KICKER TEST RESULTS

The modulator is tested into both resistive loads and into the kicker structure used on the ETA II accelerator at LLNL. The modulator has been operated at variable pulse-widths and at burst frequencies exceeding 5 MHz. All data are measurements for the pulser while driving a 50Ω load resistance. Single pulse data at 18kV and 20kV, as shown in Fig. 6 and Fig. 7, demonstrate the performance with regard to pulse waveshape and rise and fall times. The four-pulse burst in Fig. 8 demonstrates the pulsewidth agility of the modulator at variable burst frequency: the burst format is generated by an arbitrary waveform generator.

Since the output of an adder circuit is simply the sum of the individual modules, a modulation capability can be added by gating on/off modules during the voltage pulse. For example, if twenty modules are used in the stack, turning a single module gated on/off modulates the load voltage ~± 5%. In addition, if some of the modules are charged to voltages less than the standard module voltage, smaller incremental changes are possible. An example of

Figure 5. Prototype Kicker Pulser Assembly with MOSFET Carrier Boards Installed

such a modulation control is shown in Fig. 9: the amplitude modulation of the load voltage is the result of 7 modules dedicated to modulation control. The timing pattern used to control each modulation module is generated by an arbitrary waveform generator [3].

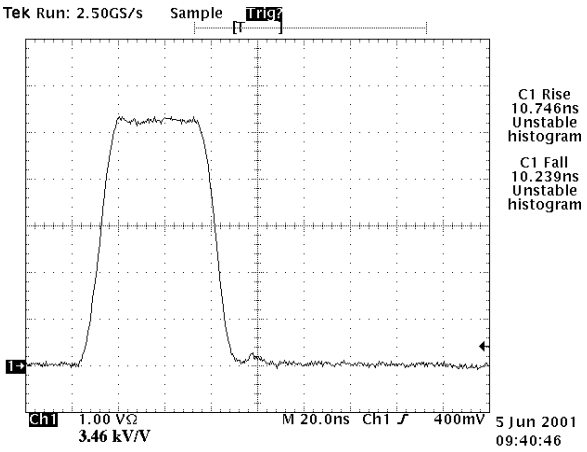

Figure 6. Single Pulse at ~ 18 kV, 30 ns Pulse Width

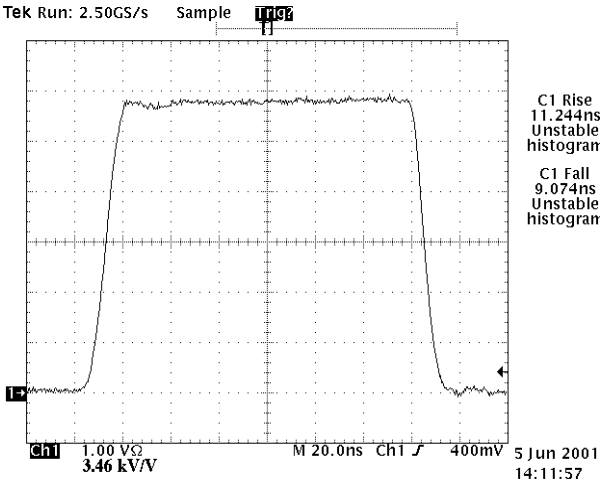

Figure 7. Single Pulse at ~20 kV, 120 ns Pulse Width

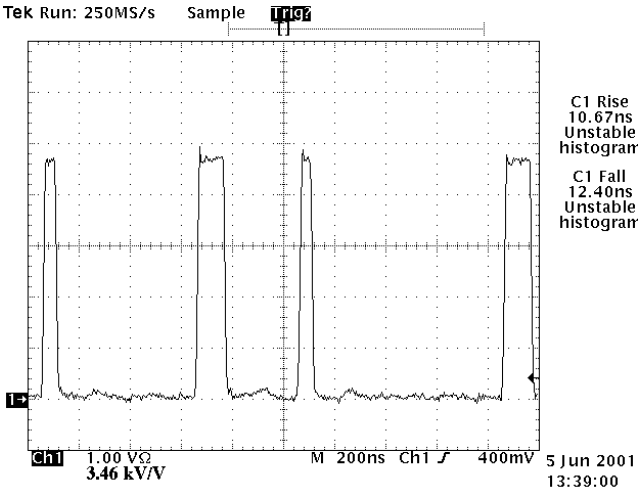

Figure 8. Four Pulse Burst at ~ 16kV – 30ns and 100ns Pulse Width

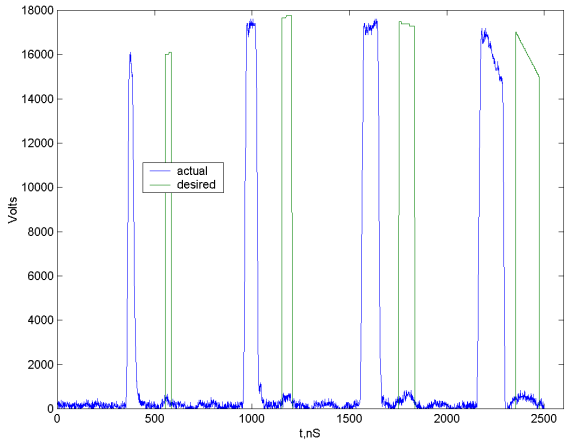

Figure 9. Four pulse burst with amplitude modulation

Figure 10 is a photograph of a complete fast dipole kicker pulser system consisting of two pulsers (one each for positive and negative 18kV), control system, diagnostics, and safety interlock system. This kicker system is also capable modulating the load voltage by ~ ±10% to within 1% of the desired voltage at the fast dipole kicker.

Figure 10.

VI. FAST EXTRACTION KICKER

A second application for a fast kicker pulser based on MOSFET switched adder technology is the extraction kicker for a 50GeV proton ring accelerator. The proton bunches (25 supported within the ring) have a center-to-center spacing of ~ 200ns. The full exploitation of the accelerator capabilities requires an asynchronous extraction kicker pulser system capable of meeting the following requirements:

Pulser Requirements

50 kV into 50 ‰ (two pulsers required to achieve –50kV)

24 pulse asynchronous burst w/max. 5 MHz burst frequency

Minimum pulse flattop - 73 ns

Maximum allowable risetime/falltime:< 64ns (0-100%)

Pulse flatness < – 1.0% for each pulse and entire burst

Intra-pulse voltage ripple - < 300V within 300ns of pulse falling edge

These requirements can be met with a pulser similar in design to the previously discussed pulser. Modifications to the design primarily involve three components: a higher current MOSFET is required, a larger value for the capacitor bank is needed to handle the voltage droop and pulse flatness requirement, and the transformer needs to be redesigned to have more volt-seconds in order to sustain the burst requirement. Initial testing to determine whether the requirements for peak voltage, risetime and falltime, pulse flattop, and intra-pulse voltage ripple could be met were performed on an extended version of the earlier described pulser (the only changes were the MOSFET used and the number of modules) (Fig. 11). A five pulse, 5MHz burst at 50 kV is shown in Fig. 12.

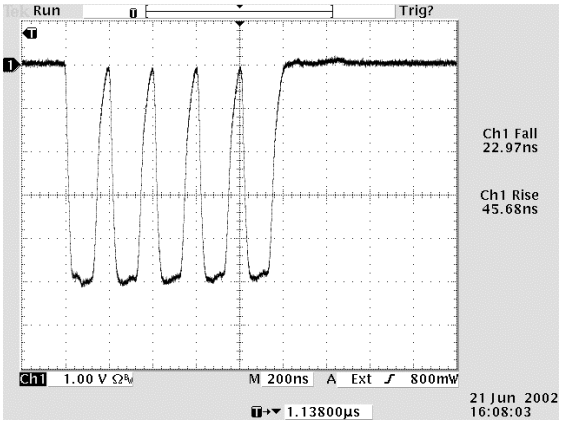

Figure 12. 5 Pulse 5MHz Burst @ 10kV/div Pulsewidth ~ 100ns (on flattop) with voltage ripple ~ ±1.2%

Figure 11. Photo of 50 kV Extraction Kicker Pulser

Design of the transformer to meet the burst requirements results in a larger structure that can support the larger magnetic core (with approximately 25 cm^2 cross-section area). As the intra-pulse voltage ripple is affected by the value of the magnetization current, several different core materials are being evaluated: Metglas™ and nanocrystalline (very low loss tape wound core).

The drive boards are redesigned to match up to the new transformer structure and to meet the voltage droop requirement. Higher current MOSFETs are also used – these devices are slightly slower than those previously used but are still capable of meeting the risetime and falltime requirements. The capacitor bank is increased approximately 10 fold from the previous design by using high energy density film capacitors. A photo of a short stack consisting of four transformers and drive boards is shown in Fig. 13.

Figure 13. A 4-cell adder stack with drive boards

A 2.125Ω load resistance is shown in the middle of the stack and is connected to the secondary (a metal rod through the middle of the transformer assembly. Measurements on this stack with two cores being driven at ~ 750 volts per cell (each by a single drive board) are shown in Figs. 14, 15, and 16. Fig. 14 shows a 34 pulse burst (pulsewidth set at ~ 150 ns) at a burst frequency of 2Mhz. The cores in this measurement are starting to saturate by the 31st pulse of the burst. Voltage droop measurements are made by examining the expanded (in time) pulse waveforms for the 1st and 20th pulses of the burst (Fig. 15 and 16). This measurement indicates that the voltage droop is approximately 2.9% over the 20 pulses which exceeds the requirement for voltage droop. As it is not practical to increase the capacitance on the drive board, this requirement can instead be met by having several spare modules in the adder stack that can be gated on as needed during the burst to compensate for the voltage droop. These pulse measurements also indicate a rolloff on the leading edge of the pulse – this is due to the L/R time constant of the modulator inductance and the 2.125Ω load resistance and will be substantially improved as the output voltage increases and the load resistance approaches the required 50Ω.

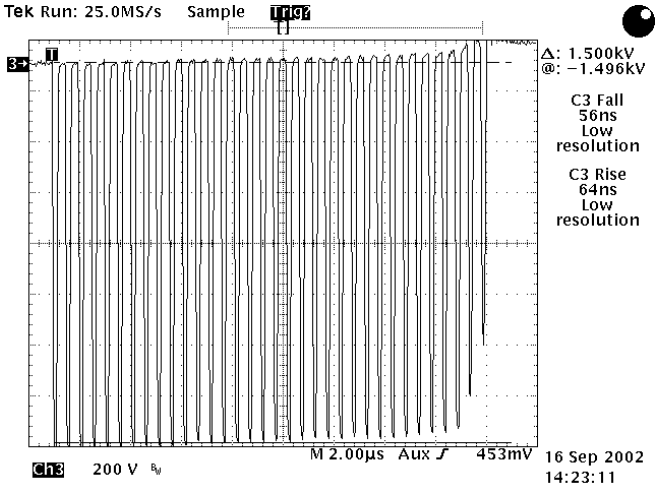

Figure 14. 34 pulse burst at 2 Mhz

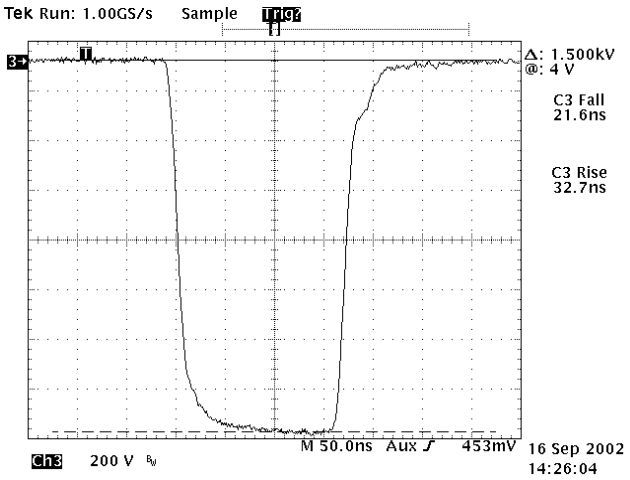

Figure 15. 1st Pulse of 34 pulse burst

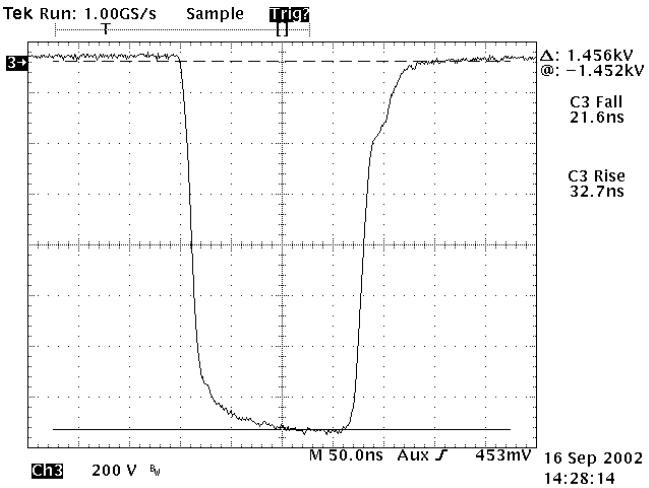

Figure 16. 20th pulse of 34 pulse burst

VII. NLC KLYSTRON PULSER

The Next Linear Collider (NLC) is a large RF linear accelerator that will require a large number of modulators to drive high-voltage high-power klystrons. The modulator requirements presented in Table 2 are substantially different from the kicker pulsers previously discussed: the peak and average power are much higher and the modulator does not operate in burst mode. The efficiency and reliability requirements effectively preclude the use of traditional PFNs and thyratrons.

Table 2. NLC Pulser Performance Requirements

Parameter	Requirement
Output Voltage/Current	-500kV @ 2kA
Pulse Width	3μs
Voltage Rise/Fall-time	~400ns
Repetition Rate	120 Hz
Peak Power	1 GW
Average Power	500kW
Lifetime	30 years

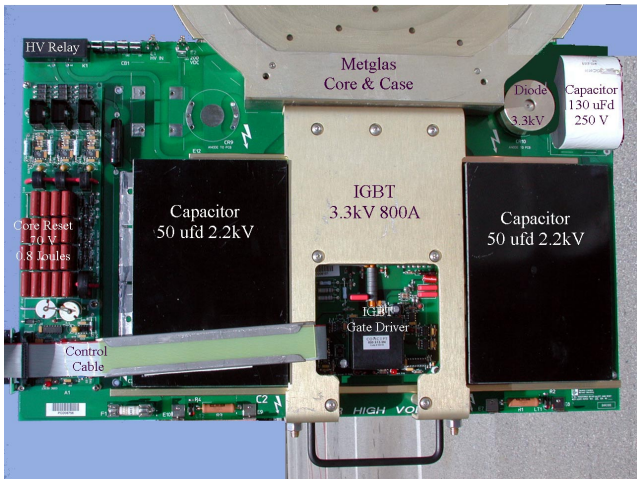

Figure 17. Drive board for NLC module

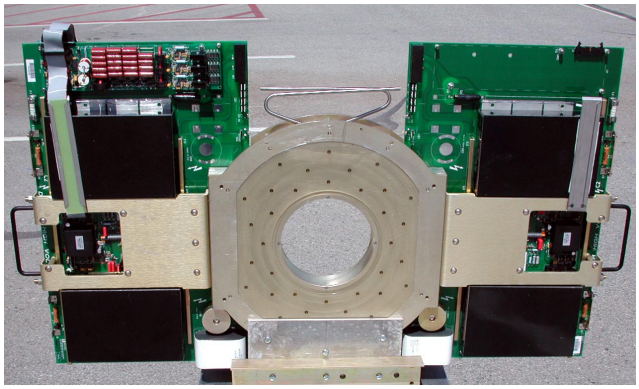

Figure 18. Complete prototype NLC Modules with transformer and two drive boards

An adder circuit that satisfies these requirements has the same topology as previously shown but the components are substantially different. The switching speed that MOSFETs are capable of is not necessary to satisfy the rise and fall time requirements and the peak current would require very large number of parallel devices. The solid-state devices that makes sense for this application are Insulated Gate Bipolar Transistors (IGBTs). High power IGBTs are available at single device operating voltages 3.3-6.5 kV with respective average currents of 1200-600 amperes. These devices are manufactured for the traction industry but testing indicates that these IGBTs may be operated at peak pulse currents of ~ 3kA and still satisfy risetime and falltime requirements when gated on/off with an appropriately designed gate drive circuit.

A prototype design for this application uses 76 modules using 3.3 kV devices operated at 2.2kV. The risetime/falltime requirements allow the use of a 3 turn secondary even though it has higher inductance. As shown in Figs. 17 and 18, each module consists of a pulse transformer and two drive boards – each board is capable of providing 3kA at 2.2 kV for the 3μs pulse duration. The modules are arranged in two vertical stacks of 38

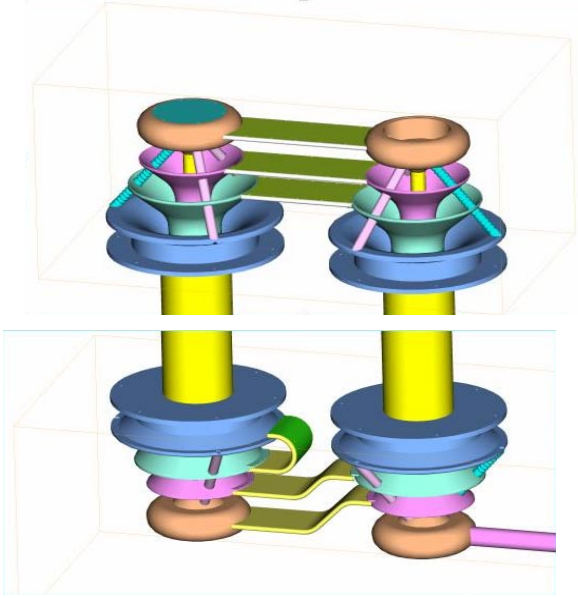

Figure 19. Three turn secondary – photo and artists' rendition

modules. The secondary turns are oil insulated concentric tubes that loop through the two stacks (Fig. 19). A photo of the complete NLC prototype modulator is shown in Fig. 20. This photo shows the modulators with a dummy load and three klystron loads. Fig. 21 is test data comparing the adder output voltage waveshape to the traditional PFN waveshape at an operating voltage of 350 kV. The overshoot seen on the adder waveshape can be corrected by time delaying the gate trigger to a few of the adder modules. Extensive testing of the prototype modulator is now in progress with functional klystrons in a dedicated test facility.

To reduce manufacturing cost, the design of the NLC modulator is undergoing a second iteration and is incorporating a higher voltage IGBT (6.5 kV) that is expected to operate at 4kV. A new transformer design will use castings for the housings and a simplified support structure for the magnetic cores. A cad drawing of the new module design is shown in Fig. 22.

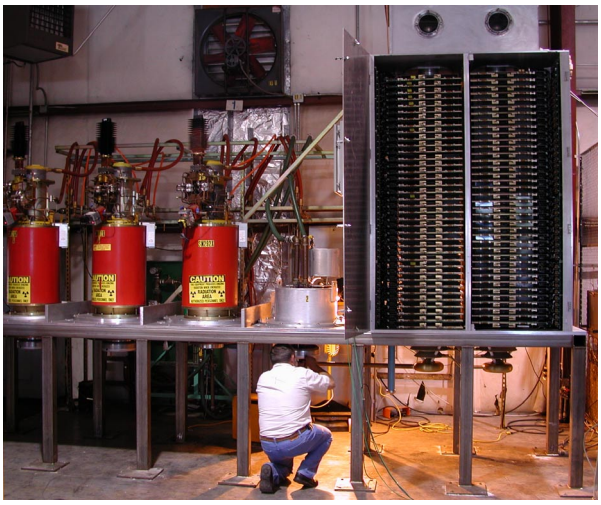

Figure 20. Complete prototype adder modulator with loads

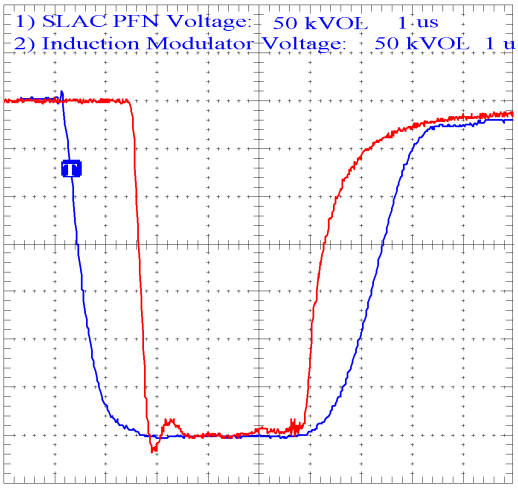

Figure 21. Comparison of adder and PFN voltage waveforms

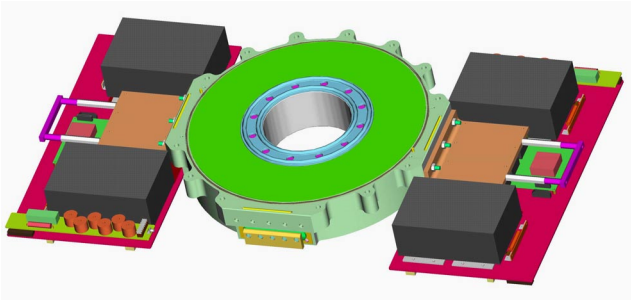

Figure 22. Drawing of new NLC module with transformer and two drive boards

VIII. SUMMARY

Modulators based on inductive voltage adder circuit topology have capabilities that cannot be easily duplicated with other pulse generation technologies. These modulators demonstrate great versatility with regard to pulse width and pulse repetition rate while maintaining fast pulse rise and fall times and are also capable of being scaled to very high output voltage and peak/average power levels.

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